

DMOS DEVICE HAVING A TRENCHED BUS STRUCTURE

ABSTRACT OF THE DISCLOSURE

A DMOS device having a trench bus structure thereof is introduced. The trench bus structure comprises a field oxide layer formed on a P substrate, and a trench extending from an top surface of the field oxide layer down to a lower portion of the P substrate. A gate oxide layer and a polysilicon bus are formed to fill the trench as a main portion of the bus structure. In addition, an isolation layer and a metal line are formed atop the polysilicon bus and the field oxide layer. An opening is formed in the isolation layer to form connections between the polysilicon bus and the metal line. In specific embodiments, the bus trench and the gate trenches of the DMOS device are formed simultaneously, and the polysilicon bus and the gate electrode are formed simultaneously as well. Therefore, the bus structure is able to form the DMOS transistor without demanding any lithographic step for defining the position of the polysilicon bus.

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